The Advantages of FLEX 10K Versus Lucent ORCA Devices

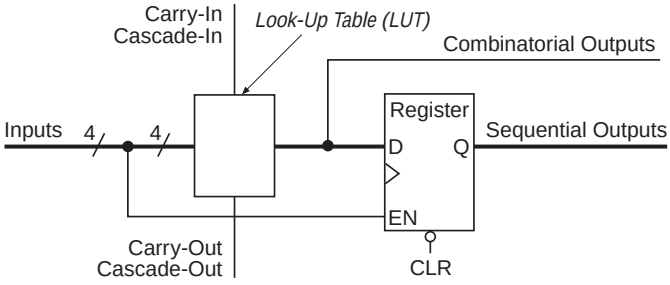
TECHNICAL BRIEF 31 OCTOBER 1997

To produce the best designs, programmable logic users focus on device density, price, performance, and availability. Compared with other high-density devices, Altera® FLEX® 10K devices offer high density, fast performance, low prices, simple routing, and a high probability of fitting. Moreover, FLEX 10K devices are available now. This technical brief evaluates the advantages of FLEX 10K devices versus Lucent ORCA devices.

Density: Avoiding the Logic-Versus-Memory Tradeoff

Comparing densities of competing devices requires an understanding of the gate counting methodologies used by each programmable logic vendor. The basic building block in Altera FLEX 10K devices is the logic element (LE), which is shown in Figure 1. Each Altera LE contains 12 usable gates.

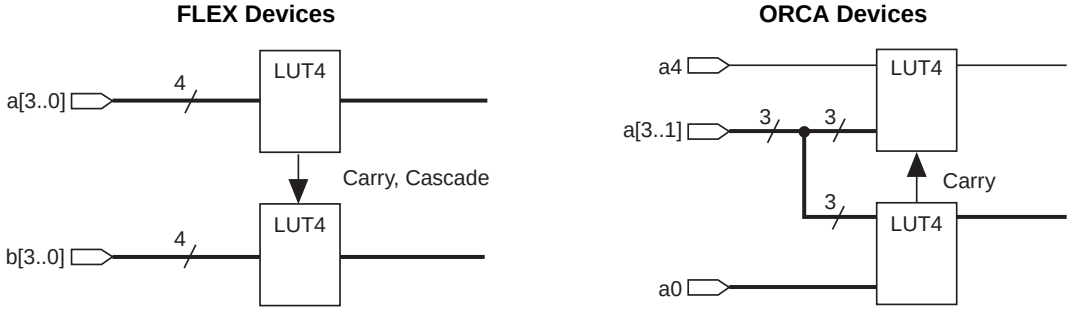
Figure 1. The FLEX Logic Element



Lucent's ORCA family uses the programmable logic cell (PLC) as its elementary architectural block. Each PLC contains a programmable function unit (PFU), which is analogous to the LE. In addition to the PFU, each PLC contains routing sources.

Figure 2 compares the two 4-input look-up tables (LUTs) in FLEX and ORCA devices. Each FLEX LUT has four independent inputs. Designers can feed adjacent two 4-input buses in adjacent LUTs. In contrast, each ORCA LUT shares three of its four inputs with the adjacent LUT. When designers utilize the second ORCA LUT for the bus `a[3..1]`, only one independent line—not a bus—can be fed into the top LUT.

Figure 2. Two 4-Input Look-Up Tables (LUTs) in FLEX and ORCA Devices



Thus, one ORCA LUT cannot perform the same functionality as one FLEX 10K LUT. Because each ORCA PFU contains four LUTs, and each FLEX LE contains one LUT, one PFU is not equal to four LEs. Originally, Lucent specified that each PFU contained 36 logic gates (Lucent Technologies *Optimized Reconfigurable Cell Array (ORCA) OR2CxxA Series Field-Programmable Gate Arrays* Preliminary Data Sheet, March 1996, pg.1). In more recent publications, Lucent has changed this specification to 48 logic gates without changes to the actual PFU (Lucent Technologies *Field-Programmable Gate Arrays Data Book*, October 1996, pg. 2-5). Altera Applications determined that one PFU performs the same functionality of three FLEX LEs (that is, 36 logic gates).

Because FLEX 10K devices have embedded RAM blocks, available logic does not decrease if a design requires RAM. The absence of embedded RAM blocks reduces the effective density of ORCA devices because available logic decreases when memory is accessed.

Performance Comparison

In the FLEX 10K architecture, connections between LEs and device I/O pins are provided by the FastTrack™ Interconnect, a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the ORCA segmented architecture complicates routing and reduces fitting probability. Table 1 shows the performance comparison between FLEX 10K and Lucent ORCA devices.

Table 1. FLEX 10K & Lucent ORCA Device Efficiency

Device	Density			Performance *(3)*		Routing
	Claimed Minimum Usable Gates *(1)*	Actual Minimum Usable Gates *(2)*	Actual Total Usable Gate Range *(3)*	t_{CO} (ns) *(4)*	Average Benchmark Frequency (MHz) *(5)*	
EPF10K20	15,000	15,000	15,000 to 63,000	6.2	71.4	Continuous
EPF10K30	22,000	22,000	22,000 to 69,000	8.5	71.4	Continuous
EPF10K40	29,000	29,000	29,000 to 93,000	8.5	71.4	Continuous
EPF10K130V	82,000	82,000	82,000 to 211,000	9.8	71.4	Continuous
2C15A 2T15A	19,200	14,400	14,400 to 40,800	10.3	55.9	Segmented
2C26A 2T26A	27,600	20,700	20,700 to 57,100	10.5	55.9	Segmented
2C40A 2T40A	43,200	32,400	32,400 to 89,300	10.8	55.9	Segmented

Notes to Table:

(1) Source: For Lucent , seeTechnologies *Optimized Reconfigurable Cell Array (ORCA) OR2CxxA Series Field-Programmable Gate Arrays* Preliminary Data Sheet, March 1996, pg. 1. For Altera, see the most current version of the FLEX 10K Programmable Logic Device Family Data Sheet. These numbers represent the sum of the logic gates coming from the Logic Element (LEs) and the logic gates from the Embedded Array Blocks (EABs). Each LE contributes with 12 usable gates; each EAB (when used purely for logic) contributes with 150 usable gates.

(2) Actual gates are calculated by Altera methodology described in this technical brief. Lucent assigns 48 gates to each PFU, instead of 36. Lucent's logic count is therefore overstated by 33 percent.

(3) Performance data refers to the fastest devices shipping at the time of this printing, i.e., -3 speed -grade FLEX 10K devices, -4 speed grade ORCA devices. For Lucent data, see ***Synario App Review***, September 9, 1996, pg. 11, and Lucent Technologies ***Field-Programmable Gate Arrays Data Book***, October 1996, pg. 2-7. For Altera, this number represents the sum of the logic gates coming from the LEs and the memory gates coming from the EABs.

(4) t_{CO} represents the clock-to-output delay. For OR2C*xx*A devices, see CLK Input Pin → Output for -4 devices in the Lucent Technologies ***Microelectronics Field-programmable Gate Arrays Data Book*** (October 1996), pages 2-150 and 2-151. For FLEX devices, Altera's ***1996 Data Book*** gives an average t_{OUTCO} of 8.5 ns. For FLEX 10KA timing, see t_{OUTCO} in the *EPF10K130V Embedded Programmable Logic Device Data Sheet Supplement*, version 2.3.

(5) The average performance is given for seven typical circuits: 8 × 8 pipelined multiplier, 8 × 8 non-pipelined multiplier, 16 × 16 pipelined multiplier, 16 × 16 non-pipelined multiplier, 256 × 8 RAM (registered inputs and outputs, 32 × 16 RAM (single ports, registered inputs and outputs), and 32 × 16 RAM (dual port, registered inputs and outputs). For Lucent data, see ***Synario App Review***, September 9, 1996, pg. 11, and Lucent Technologies ***Field-Programmable Gate Arrays Data Book***, October 1996, pg. 2-7.

The documents listed below provide more detailed information. Part numbers are in parentheses.

- *FLEX 10K Embedded Programmable Logic Family Data Sheet* (A-DS-F10K-02)
- *Gate Counting Methodology for Altera's FLEX 10K Family of Embedded Programmable Logic* (M-WP-GAEPLF-01)

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